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REMARKS

Claims 1-20 are all of the claims presently pending in the present Application. Claims 1, 6 and 15 have been amended to more particularly define the invention. Claims 15-20 have been withdrawn from consideration.

It is noted that the claim amendments herein are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicants' intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Applicant gratefully acknowledges the Examiner's indication that claims 9-11 and 13-14 would be allowable if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable.

Claims 1-8 and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fujikawa et al. (U.S. Patent No. 6,323,120).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as recited in claim 1) is directed to a wiring structure for semiconductor device, which includes a wiring layer that includes copper as main component, and a crystal grain promotion layer that contacts said wiring layer and promotes enlargement in a crystal grain of the wiring layer.

Conventional wiring structures using a copper wiring are typically formed by a Damascene process in which a barrier layer is formed in a trench of a substrate, and the copper wiring is formed on the barrier layer (Application at Figure 1B; page 2, line 7 -page 3, line 20). However, the barrier layer must be thick which causes it to increase the resistivity of the wiring.

The claimed invention, on the other hand, includes a crystal grain promotion layer that

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contacts said wiring layer and promotes enlargement in a crystal grain of the wiring layer (Application at page 8, lines 5-21). The inventors found that the size of the crystal grain of the wiring layer may be enlarged by the existence of the crystal grain promotion layer, and therefore, a wiring (e.g., a nano-scale copper wiring) having a low resistivity and high reliability can be realized (Application at page 4, lines 23-25; page 6, lines 5-6).

II. THE RESTRICTION REQUIREMENT

The Examiner alleges that claims 15-20 are directed to an invention which is distinct from the invention of claims 1-14. Specifically, the Examiner alleges that "the method can be used to form a wiring layer containing copper as a minor component rather than a main component".

Applicant notes that claim 15 has been amended to recite "*forming a wiring layer comprising copper as a main component on said promoting layer...*".

In view of the foregoing, the Examiner is respectfully requested to withdraw this restriction requirement and examine claims 1-20 in this Application.

III. FUJIKAWA

The Examiner alleges that Fujikawa teaches the claimed invention of claims 1-5. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Fujikawa.

Fujikawa discloses a method of forming a wiring film, which includes forming a barrier layer 3 on an insulation film 2 having a hole 2A, forming a copper seed layer on the barrier layer and laminating a wiring film 5A by electrolytic plating, and heat treating the structure at high temperature and pressure (Fujikawa at Abstract).

However, contrary to the Examiner's allegations, Fujikawa does not teach or suggest "*a crystal grain promotion layer that contacts said wiring layer and promotes enlargement in a crystal grain of the wiring layer*", as recited, for example, in claim 1.

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As noted above, the inventors found that the size of the crystal grain of the wiring layer may be enlarged by the existence of the crystal grain promotion layer, and therefore, a wiring (e.g., a nano-scale copper wiring) having a low resistivity and high reliability can be realized (Application at page 4, lines 23-25; page 6, lines 5-6).

Clearly, these novel features are not taught or suggested by Fujikawa. Indeed, the Examiner attempts to equate the barrier layer 3 in Fujikawa with the crystal grain promotion layer in the claimed invention. This is clearly unreasonable.

First, Applicant would point out that in Fujikawa, the barrier layer 3 is formed on the oxide film 2 and silicon wafer 1, and the seed layer 4 is formed on the barrier layer 3 (Fujikawa at col. 4, lines 1-26; Figures 1(a), 1(b)). The wiring film 5 is then formed on the seed layer 4, not on the barrier layer 3. That is, the wiring film 5 clearly does not contact (e.g., physically contact) the barrier layer 3 in Fujikawa.

Indeed, Applicant would point out that the function of the barrier layer 3 in Fujikawa is "for preventing copper from diffusing to the insulation film 2 or Si in the substrate 1 by a CVD process or a PVD method such as sputtering" (Fujikawa at col. 4, lines 7-10). That is, nowhere does Fujikawa state either expressly or implicitly, that the barrier layer 3 may promote enlargement in a crystal grain of the wiring film 5. Indeed, Applicant would respectfully submit that it is very unlikely that the barrier layer 3 could even have such a function since the barrier layer 3 does not contact the wiring film 5, but is separated from the wiring film 5 by the seed layer 4 which is intended to seed the growth of the wiring film 5.

In fact, nowhere does the Examiner indicate where Fujikawa makes any association between the barrier layer 3 and the size of the crystals in the wiring film 5. Applicant submits that if the Examiner continues to maintain this rejection, the Examiner must indicate in detail where Fujikawa associates the barrier layer 3 and the size of the crystals in the wiring film 5.

Indeed, the Examiner merely states that Fujikawa states that "the wiring layer 5 has a larger than normal crystal grain size". However, this has nothing to do with the barrier layer 3. In fact, Fujikawa refers to Figure 1a and states that when a heat treatment is applied "in a highly

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pressurized gas atmosphere", growing of crystal grains is promoted and a wiring film 5A having a larger crystal grain size compared with that of the wiring film generally heat treated **at an atmospheric pressure** can be obtained (Fujikawa at col. 4, lines 52-62) (emphasis added). That is, Fujikawa merely teaches that a grain size of the wiring film may be larger at a higher pressure than at atmospheric pressure.

Therefore, it is completely unreasonable to attempt to equate the barrier layer 3 in Fujikawa with the crystal grain promotion layer of the claimed invention, that contacts the wiring layer and promotes enlargement in a crystal grain (e.g., promotes enlargement of the size of the crystal grain) of the wiring layer.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggested by Fujikawa. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.


Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,


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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing was filed by facsimile with the United States Patent and Trademark Office, Examiner Roy Karl Potter, Group Art Unit # 2822 at fax number (571) 273-8300 this 18th day of October, 2005.


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